UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,120	07/16/2003	Chih Yuan Huang	MXIC 1532-1	1938

22470 7590 09/29/2004

HAYNES BEFFEL & WOLFELD LLP
P O BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,120	HUANG ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-11** are currently pending in this application is acknowledged.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 07/16/2003 and made of record as Paper No. 092304. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claim **8** is objected to because of the following reasons.

Claim **8** should be dependent from independent claim **7** instead of claim **6**.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-6** are rejected under 35 U.S.C. 102(b) as being anticipated by Griswold (USP: 4,748,133).

Regarding claim **1**, Griswold discloses in Fig. 8 and the corresponding texts as set forth in column 2, line 19-column 3, line 45, a multi-layer assembly comprises:

a first silicon layer (combination of layers 18 and 20) comprising at least first and second surfaces, and further comprising a structure (combination of layers 18 and 20) that transitions from an amorphous silicon region (20) adjacent to the first surface, to a polysilicon region (18) adjacent to the second surface;

a second layer/a second oxide layer (28) adjacent to the first surface of the first layer; and

a third layer/a first oxide layer (16) adjacent to the second surface of the first layer; wherein at least one of the second and third layers comprises a dielectric.

Regarding claims **2-3**, Griswold discloses in Fig. 8 and the corresponding texts as set forth in column 2, line 19-column 3, line 45, a multi-layer assembly comprises:

a first silicon layer (combination of layers 18 and 20) comprising at least first and second surfaces, and further comprising a structure (combination of layers 18 and 20) having a first region composed of amorphous silicon (20) adjacent to the first surface, a second region composed of polysilicon (18) adjacent to the second surface, and an intermediate region (the interface between layers 18 and 20) between the first and second regions, the intermediate region comprised partially of amorphous silicon and partially of polysilicon;

a second layer/a second oxide layer (28) adjacent to the first surface of the first lAyer; and

a third layer/a first oxide layer (16) adjacent to the second surface of the first layer; wherein at least one of the second and third layers comprises a dielectric.

Regarding claim **4**, Griswold discloses in Fig. 8 and the corresponding texts as set forth in column 2, line 19-column 3, line 45, a semiconductor device having a floating gate (22), the floating gate comprises a silicon structure (combination of layers 18 and 20) having at least first and second surfaces and transitioning from an amorphous silicon region (20) adjacent to the first surface to a polysilicon region (18) adjacent to the second surface.

Regarding claims **5-6**, Griswold discloses in Fig. 8 and the corresponding texts as set forth in column 2, line 19-column 3, line 45, a semiconductor device having a floating gate (22), the floating gate comprises a silicon structure (combination of layers 18 and 20) having at least first and second surfaces;

the structure comprises at least first (20) and second regions (18);

the first region comprising amorphous silicon (20), and adjacent to the first surface;

the second region comprising polysilicon (18), and adjacent to the second surface; and wherein the silicon structure further comprises an intermediate region (the interface between layers 18 and 20) between the first and second surfaces, wherein the intermediate region has a phase distribution that transitions from amorphous silicon to polysilicon.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **7-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Griswold (USP: 4,748,133) in view of Liaw et al. (USP: 4,963,506 hereinafter referred to as "Liaw"), Applicant submitted prior art (ASPA).

Regarding claims **7-8**, Griswold discloses in Fig. 8 and the corresponding texts as set forth in column 2, line 19-column 3, line 45, a method of forming a layer on a substrate (10), comprises:

depositing a silicon layer (combination of polysilicon layer 18 and amorphous silicon layer 20) on the substrate.

Griswold does not disclose a method of forming a layer on a substrate (10) comprises controlling the temperature during the step of depositing the silicon layer, from a starting temperature favoring the formation of polysilicon, to an ending temperature favoring the formation of amorphous silicon, and wherein the starting temperature is approximately 620°C; and the ending temperature is in a range from about 500°C to about 550°C.

Liaw teaches that for the deposition of amorphous silicon, the temperature should be in the range of approximately 200 to 550 degrees centigrade, and for the deposition of polycrystalline silicon, the temperature should be in the range of approximately 550 to 750 degrees centigrade as set forth in column 3, lines 1-10.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the temperature in the range of approximately 550 to 750 degrees centigrade as a starting temperature to form polysilicon silicon layer and the temperature in the range of approximately 200 to 550 degrees centigrade as an ending temperature to form amorphous

silicon layer, as taught by Liaw in order to control the temperature range during the step of depositing polysilicon layer and amorphous silicon to arrive the claimed limitations.

Regarding claims **9-11**, Griswold discloses in Fig. 8 and the corresponding texts as set forth in column 2, line 19-column 3, line 45, a method of forming a floating gate (22) on a semiconductor substrate (10), comprises:

forming a first dielectric layer/a first oxide layer (16) on the semiconductor substrate;

depositing a silicon layer (combination of polysilicon layer 18 and amorphous silicon layer 20) superposing the first layer/the first oxide layer;

forming a second dielectric layer/a second oxide layer (28) superposing the silicon layer.

Griswold does not disclose a method of forming a floating gate on a semiconductor substrate, comprises controlling the temperature during the step of depositing the silicon layer, from a starting temperature to an ending temperature, wherein the starting temperature is higher than the ending temperature, wherein the starting temperature is selected to form a polysilicon region adjacent to the first dielectric layer; and the ending temperature is selected to form an amorphous silicon region adjacent to the second dielectric layer; and wherein the starting temperature is approximately 620°C; and the ending temperature is in a range from about 500°C to about 550°C.

Liaw teaches that for the deposition of amorphous silicon, the temperature should be in the range of approximately 200 to 550 degrees centigrade, and for the deposition of polycrystalline silicon, the temperature should be in the range of approximately 550 to 750 degrees centigrade as set forth in column 3, lines 1-10.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the temperature in the range of approximately 550 to 750 degrees centigrade as a starting temperature to form polysilicon silicon layer adjacent to the first dielectric layer/the first oxide layer and the temperature in the range of approximately 200 to 550 degrees centigrade as an ending temperature to form amorphous silicon layer adjacent to the second dielectric layer/the second oxide layer in which the starting temperature is higher than the ending temperature, as taught by Liaw in order to control the temperature range during the step of depositing polysilicon layer and amorphous silicon to arrive the claimed limitations.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

09/23/04

Andy Huynh

Patent Examiner